WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a dielectric layer defining at least one aperture therein;

a barrier layer formed along the bottom and side walls of said at least one aperture;

a high temperature superconductor (HTS) layer formed over the barrier layer in said at least one aperture; and

a conductive material filling said aperture in said dielectric layer.

2. The semiconductor device of claim 1 wherein the dielectric layer is a low-k dielectric material.

3. The semiconductor device of claim 1 wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.

4. The semiconductor device of claim 3 further comprising a tantalum layer over the HTS layer.

5. The semiconductor device of claim 1 wherein the barrier layer comprises a layer of a tantalum-rich nitride over the HTS layer, and further comprising a layer of tantulum.

6. The semiconductor device of claim 1 wherein the HTS material is a rare earth cuprate (copper oxide) material.

7. The semiconductor device of claim 1 wherein the HTS material is a rare earth element combined with barium copper oxide.

8. The semiconductor device of claim 7 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

9. The semiconductor device of claim 7 wherein the HTS material is yttrium barium copper oxide.

10. The semiconductor device of claim 1 wherein said HTS layer is a rare earth Ruthenium Oxocuprate.

11. The semiconductor device of claim 10 wherein said rare earth Ruthenium Oxocuprate is defined by the formula $RuSr_x$ (rare earth element) Cu_yO_z in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45, and z is between about 7.55 and 8.45.

12. The semiconductor device of claim 11 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

13. The semiconductor device of claim 1 wherein the HTS layer has a thickness of between 10 Å to 500 Å.

14. The semiconductor device of claim 1 wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.

15. The semiconductor device of claim 1 wherein the aperture defined in said dielectric has a width less than about 300 Å.

16. The semiconductor device of claim 3 wherein the aperture defined in said dielectric has a width less than about 300 Å.

17. The semiconductor device of claim 1 wherein said at least one aperture includes at least two trenches.

18. The semiconductor device of claim 17 wherein one of said at least two trenches further includes a via.

19. The semiconductor device of claim 1 further comprising a capping layer over said conductive metal filling said at least one aperture.

20. The semiconductor device of claim 19 wherein said capping layer is an HTS capping layer.

21. The semiconductor device of claim 19 further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.

22. The semiconductor device of claim 19 further including a hard mask over said HTS capping layer.

23. The semiconductor device of claim 22 wherein said hard mask is a layer of ARC.

24. The semiconductor device of claim 21 wherein said HTS capping layer has a thickness between about 10 Å and 500 Å.

25. A semiconductor device comprising:

a first dielectric layer defining at least one aperture therein;

a conductive material filling said at least one aperture in said first dielectric layer;

an HTS capping layer over said conductive material filling said at least one aperture; and

another dielectric layer over said first dielectric layer and said HTS capping layer.

26. The semiconductor device of claim 25 wherein said HTS capping layer has a thickness of between about 10 Å and 500 Å.

27. The semiconductor device of claim 25 wherein said aperture in said first dielectric layer has a width less than about 300 Å

28. The semiconductor device of claim 25 wherein the HTS material is a rare earth cuprate (copper oxide) material.

29. The semiconductor device of claim 25 wherein the HTS material is a rare earth element combined with barium copper oxide.

30. The semiconductor device of claim 29 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

31. The semiconductor device of claim 29 wherein the HTS material is yttrium barium copper oxide.

32. A method of making a semiconductor device comprising the steps of:

forming a dielectric layer over a substrate;

defining at least one aperture in said dielectric layer;

forming a barrier layer on the bottom and sidewalls of said at least one aperture;

forming a high temperature superconductor (HTS) layer over said barrier layer; and depositing a conductive material in said at least one aperture defined in said dielectric layer.

33. The method of claim 32 wherein the dielectric layer is a low-k dielectric material.

34. The method of claim 32 wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations thereof.

35. The method of claim 33 wherein the barrier layer comprises a layer of tantalum, and further comprising a layer of tantalum over said HTS layer.

36. The method of claim 32 wherein the HTS material is a rare earth cuprate (copper oxide) material.

37. The method of claim 32 wherein the HTS layer is a rare earth element combined with barium copper oxide.

38. The method of claim 37 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

39. The method of claim 37 wherein the HTS layer is yttrium barium copper oxide.

40. The method of claim 32 wherein said HTS layer is a rare earth Ruthenium Oxocuprate.

41. The method of claim 40 wherein said rare earth Ruthenium Oxocuprate is defined by the formula $RuSr_x$ (rare earth element) Cu_yO_z in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45 and z is between about 7.55 and 8.45.

42. The method of claim 40 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

43. The method of claim 32 wherein the HTS layer has a thickness of from 10 Å to 500 Å.

44. The method of claim 32 wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.

45. The method of claim 32 wherein said at least one aperture has a width less than 300 Å.

46. The method of claim 32 further comprising the step of forming a capping layer over said conductive material deposited in said aperture defined in said dielectric.

47. The method of claim 46 wherein said step of forming said capping layer comprises forming a patterned hard mask over a layer of HTS material.

48. The method of claim 46 wherein said step of forming a capping layer comprises forming a layer of HTS.

49. The method of claim 48 wherein said HTS capping layer is formed to a thickness of between 10 Å and 500 Å.

50. The method of claim 48 comprising the further step of depositing another dielectric layer over said dielectric layer and said HTS capping layer.

51. A method of making a semiconductor device comprising the steps of:

forming a dielectric layer over a substrate;

defining at least one aperture in said dielectric layer;

depositing a conductive material in said at least one aperture defined in said dielectric layer; and

forming an HTS capping layer over said conductive material deposited in said aperture.

52. The method of claim 51 wherein said step of forming an HTS layer comprises the step of forming said HTS layer to a thickness of between about 10 Å and 500 Å.

53. The method of claim 51 wherein the HTS material is a rare earth cuprate (copper oxide) material.

54. The method of claim 51 wherein the HTS material is a rare earth element combined with barium copper oxide.

55. The method of claim 54 wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.

56. The method of claim 54 wherein the HTS material is yttrium barium copper oxide.